# [April-18]

**[EEC-346]**

**B.Tech. Degree Examination**

**Electronics &Communication Engineering VI SEMESTER**

**DIGITAL DESIGN WITH VERILOG**

(Effective from the admitted batch 2015–16)

Time: 3 Hours Max.Marks: 60

**Instructions:** Each Unit carries 12 marks.

Answer all units choosing one question from each unit. All parts of the unit must be answered in one place only. Figures in the right hand margin indicate marks allotted.

# MODULE-I

1. a) Explain different levels of design description in Verilog 6
   1. Explain the Simulation and Synthesis in Verilog HDL 6

# OR

1. Predict system tasks and data types in Verilog HDL. Explain 12

# MODULE-II

1. Explain about net, gate and tri-state delays with examples and

Verilog code 12

# OR

1. a) Explain blocking and Non-blocking statements with examples 6
   1. List out and explain all loop statements in behavior level with examples 6

# MODULE-III

1. a) Explain about CMOS switch and Bi-directional gates related to switch level modeling in Verilog HDL 6
   1. Explain combining assignment and net declaration with examples 6

# OR

1. a) Design a half subtractor using CMOS Switches 6
   1. State the rules to be followed to declare and to use the

bi-directional lines 6

# MODULE-IV

1. a) Explain dice game with block diagram 6
   1. Illustrate the concept of state machine charts 6

# OR

1. a) Explain the realization of SM chart 6
   1. Design state graph for Dice game controller 6